

Finest Schemes for Jitter and Power Optimization with Improved Performance Strategy of N-PLL using Gwo Algorithm

Kokila S, Vijayanthi P

P.G. Student, Department of Electronics and Communication Engineering, Gnanamani College of Technology,
Namakkal, Tamil Nadu, India

Assistant Professor, Department of Electronics and Communication Engineering, Gnanamani College of Technology,
Namakkal, Tamil Nadu, India

ABSTRACT: In the modern technological world, information and communication devices and their technology are moving towards a new chapter day by day. Especially after the advent of digital communication, information is handled at a high speed and with great security. In digital communication system, a clock recovery system plays major role which extracts timing information from a data stream for accurate bit-level decoding, essential in communications process. A frequency synthesizer generates stable, precise frequencies for various applications, such as tuning radios, mobile phones, and tracking systems like GPS etc. While distinct, some advanced circuits can perform both functions, using a phase-locked loop (PLL) to recover a clock and also generate frequencies. This system proposes a Grey Wolf Optimization (GWO) algorithm based jitter and power optimization in a Phase-Locked Loop (N-PLL) design. GWO is a metaheuristic algorithm widely applied to complex, non-linear engineering optimization problems where finding optimal design parameters are challenging for traditional methods.

KEYWORDS: Grey wolf optimization algorithm (GWO), Minimization of jitter in N-PLL.

I. INTRODUCTION

In modern digital integration system design such as ASIC design, Smartphone chips and MEMS plays major role in all commercial instruments. The performance of the digital systems is based on clock frequency. High-performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. This research presents innovative techniques at both system and circuit levels that minimize the clock timing uncertainty with minimum power and area overhead. A PLL is essentially a feedback loop that locks the on-chip clock phase to that of an input clock or signal. Because the on-chip clock toggles a large capacitive load, a series of clock buffers efficiently increases the drive strength of the PLL output to drive the load. High-performance PLLs and clock buffers are widely used within a digital system for two purposes: clock generation, and timing recovery. For clock generation, since off-chip reference frequencies are limited by the maximum frequency of a crystal frequency reference¹, a PLL receives the reference clock and multiplies the frequency to the multi-gigahertz operating frequency. The research also represents a powerful noise-filtering technique that minimizes jitter through adjusting the key loop parameters of a PLL based on the dominant noise source in the PLL. The power performance of a PLL is a growing concern for many applications. Power dissipated by PLLs is often a small fraction of the total active power.

II. LITERATURE SURVEY

As phase-locked loop (PLL) architectures become increasingly complex, optimizing the jitter and power performance through calculation alone is becoming more challenging for fractional-N PLLs. [1] To find the most suitable PLL architecture that meets the jitter-power requirements of various applications, a simple and widely-applicable method is in demand to find the optimal jitter-power relation of different PLL architectures. In this paper, we propose the use of a multi-objective evolutionary algorithm (MOEA) to optimize the jitter and power of PLLs, specifically focusing on two popular fractional-N PLL architectures: digital-to-time converter (DTC)-based and harmonic-mixer (HM)-based PLLs.

By applying the MOEA, we can achieve optimal jitter and power relationships for both architectures and the observed trends in jitter and power are explained and supported with calculations. [2] A grid-tied inverter needs excellent maximum power point tracking (MPPT) topology to extract the maximum energy from PV panels regarding energy creation. An efficient MPPT ensures that grid codes are met, maintains power quality and system reliability, minimizes power losses, and suppresses rapid response to power fluctuations due to solar irradiance. Moreover, appropriate MPPT enhances economic returns by increasing energy royalties and ensures high power quality with reduced harmonic distortion.[3] This work presents the design and analysis of phase-locked loops (PLLs) tailored for high performance frequency and phase control applications. These PLLs are essential in systems requiring precise frequency synthesis, phase-aligned clock generation, and robust phase synchronization, particularly in wireless communication systems, RF front-ends, and high-speed data converters.

III. METHODOLOGY

The system design focused towards directly linking Grey Wolf Optimization (GWO) to N-PLL (Fractional-N or Integer-N Phase-Locked Loop) jitter optimization in a singular, established methodology is not widely documented in the provided search results, GWO has been successfully applied to optimize controller parameters (such as PID or loop filter settings) in various control systems, including those involving PLLs. The fundamental principle involves using the GWO algorithm to tune the PLL's design parameters (e.g., loop bandwidth, damping factor, loop filter components) to minimize a defined objective function, which in this case would be the output jitter. The goal is to minimize the output jitter (or phase noise, which is equivalent in the time domain). The objective function should mathematically represent the jitter performance, likely incorporating factors like loop bandwidth, damping factor, and noise contributions from various components (VCO, reference clock, charge pump, power supply noise).

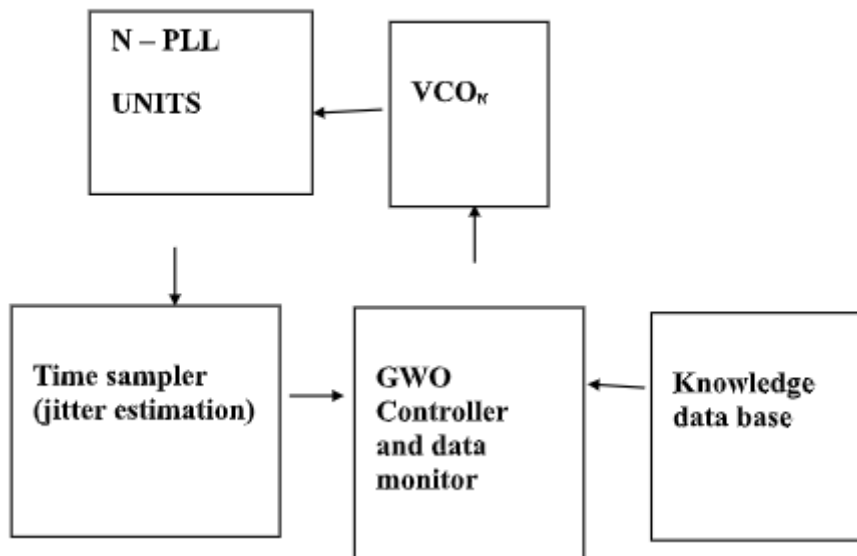


Figure3.1. Functional block diagram

The GWO algorithm would adjust key PLL design parameters. These typically include: Loop Filter Components: Resistor and capacitor values that determine the loop bandwidth and damping factor. VCO Gain: In some adaptive systems, the VCO gain might be a tunable parameter. Charge Pump Current: The current levels also influence loop dynamics. A simulation model of the N-PLL (e.g., in a mixed-signal simulation environment) is required to evaluate the jitter performance for a given set of parameters provided by the GWO algorithm. Jitter and power optimization in N-PLL units using the Grey Wolf Optimizer (GWO) algorithm involves using the GWO to find the best settings for digital circuits to maintain voltage stability and minimize power loss. The algorithm, inspired by the hunting behavior of grey wolves, simulates their social hierarchy to search for optimal solutions, and improved versions

have been developed to enhance its efficiency. GWO is a simple yet efficient metaheuristic algorithm that can be effective for complex, multi-modal optimization problems where traditional analytical methods may be challenging. This approach could potentially achieve a better balance between jitter and other performance metrics (like power consumption or locking time) compared to manual design.

IV. EXPERIMENTAL RESULTS

Timing jitter has been the subject of numerous studies which provide many models to predict the jitter of individual blocks in a PLL, in particular, different types of voltage controlled oscillators (VCOs) due to device noise and supply/substrate noise. While most of previous work focuses on jitter study of individual blocks, there has been done less work on modeling the overall jitter at PLL output clock shown in simulation output (Fig.4.4). This research extends the previous work by investigating the effect of PLL parameters such as bandwidth and damping factor toward minimizing output clock jitter for various noise sources using grey wolf optimization algorithm. The proposed system model is testing and implemented in simulink model by using PROTEUS 7. The noise sources of PLL introduces the timing jitter and it reduced by using the grey wolf algorithm based optimizer. In the simulation consists of different PLL circuit using CD 4046, P-MOS and N-MOS based phase detector, ATmega328 based GWO optimizing controller and 2X16 Digital display shown in fig.4.1.

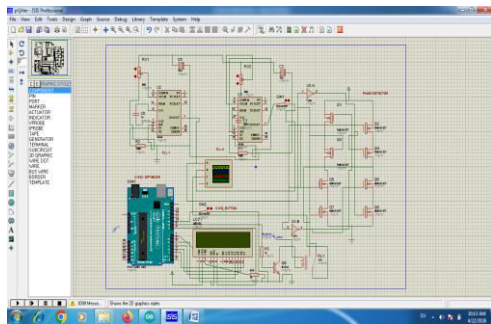


Fig. 4.1 simulation design window of the system

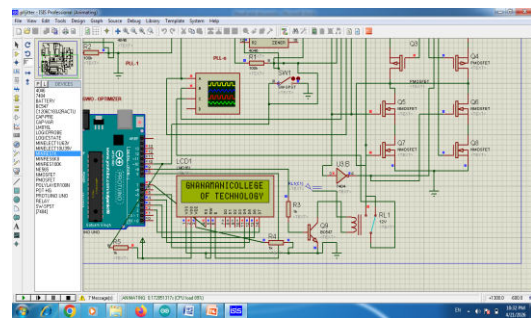


Fig. 4.2 simulation execution window of the system

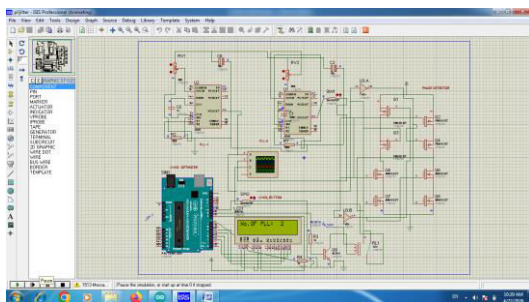


Fig. 4.3 Simulation: Multiple PLL presents

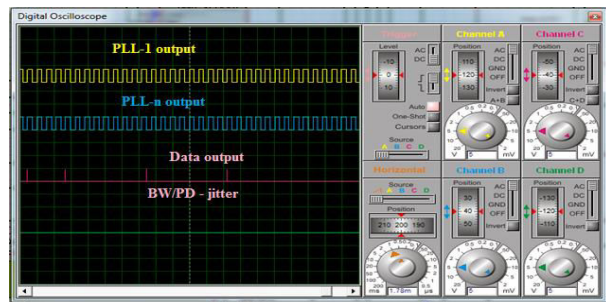


Fig.4.4 Simulation: Output of PLL-1 & 2 – jitter introduced, Bandwidth and phase shift of the Data varied

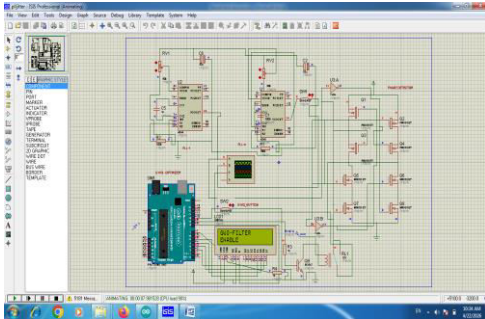


Fig. 4.5 Simulation: GWO filter activation

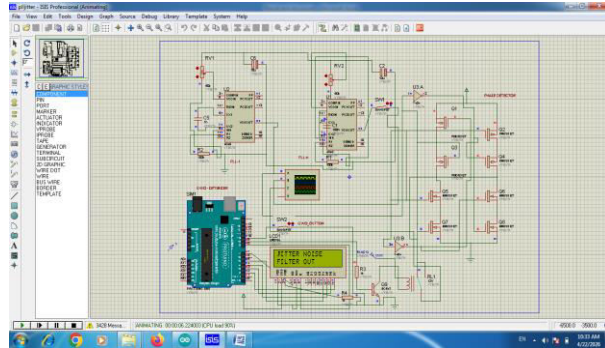


Fig. 4.6 Simulation: Reduced jitter and finest data output

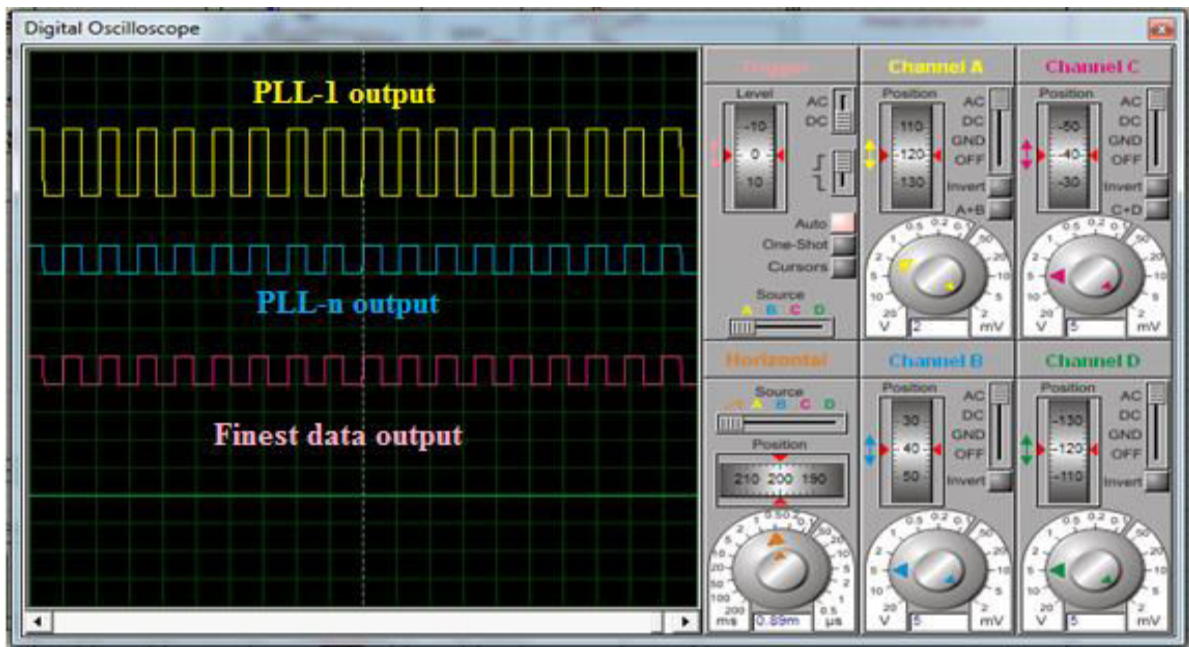


Fig. 4.7 Simulation output: Zero jitter and finest data output

V. CONCLUSION

Optimizing the N-PLL jitter involves reducing a range of design parameters, including loop bandwidth, damping factor, VCO performance, and power supply noise rejection. Proper reference clock selection, loop filter design, and deign layout further enhance jitter performance. By carefully addressing these parameters, engineers can ensure reliable and robust PLL operation tailored to specific application requirements. The minimizing of the jitter in N-PLL design and improving the better performance of the system is going to analyze by using Grey wolf Optimization algorithm. GWO is a simple yet efficient metaheuristic algorithm that can be effective for complex, multi-modal optimization problems where traditional analytical methods may be challenging. This approach could potentially achieve a better balance between jitter and other performance metrics (like power consumption or locking time) compared to manual design. The fundamental principle involves using the GWO algorithm to tune the PLL's design parameters (e.g., loop bandwidth, damping factor, loop filter components) to minimize a defined objective function, which in this case would be the output jitter. Using GWO to dynamically adjust charge-pump current, loop filter bandwidth, and divider ratios can simultaneously push jitter down while keeping power consumption low.

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